CLAIMS

1. An integrated circuit comprising:

a plurality of pixel circuits arranged in rows and columns;

a plurality of first lines, each first line connected to a corresponding column of pixel circuits; and

a plurality of second lines, each second line connected to a corresponding row of pixel circuits,

wherein the plurality of first lines are formed such that each first line extends over the plurality of second lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each first line from the plurality of second lines.

2. The integrated circuit according to Claim 1, wherein each pixel circuit includes an access transistor and a pixel element, wherein the access transistor includes a gate terminal connected to and associated first line, a first terminal connected to the pixel element, and a second terminal connected to an associated second line.

3. The integrated circuit according to Claim 2, wherein the access transistor comprises one of amorphous silicon and polysilicon.

4. The integrated circuit according to Claim 2, wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor.

5. The integrated circuit according to Claim 2, wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated second line by a buried insulator layer comprising a resin derived from B-staged bisbenzocyclobutene monomers.

6. The integrated circuit according to Claim 2, wherein the integrated circuit comprises a medical image sensor array.

7. The integrated circuit according to Claim 2, wherein each pixel element comprises an amorphous silicon sensor, and each pixel circuit further comprises a phosphor converter located over the amorphous silicon sensor.

8. An image sensor array comprising:

a plurality of pixel circuits arranged in rows and columns, each pixel circuit including an access transistor;

a plurality of gate lines, each gate line connected to the access transistors of a corresponding column of pixel circuits; and

a plurality of data lines, each data line connected to the access transistors of a corresponding row of pixel circuits,

wherein the plurality of data lines are formed such that each data line overlaps the plurality of gate lines at corresponding crossover locations, and

wherein an air-gap is defined at each crossover location that separates each data line from the plurality of gate lines.

9. The image sensor array according to Claim 8,

wherein the plurality of gate lines are formed from a first metal layer, the plurality of data lines are formed from a second metal layer such that the data lines are located above the first metal layer, wherein each of the plurality of pixel circuits also comprises a sensor including an amorphous silicon (a-Si:H) layer formed on a metal plate, and

wherein the metal plate is formed from a third metal layer formed after the first and second metal layers.

10. The image sensor array according to Claim 8, further comprising a strengthening insulator formed on the plurality of data lines at the crossover locations.

11. A method for making an integrated circuit including a plurality of first lines, a plurality of second lines, and a plurality of pixel circuits arranged in rows and columns, each column of pixel circuits being connected to a corresponding first line, and each row of pixel circuits being connected to a corresponding second line, wherein the method comprises:

forming the plurality of first lines;

forming a release material pattern over the first lines;

forming the plurality of second lines such that each data line extends over the plurality of first lines at corresponding crossover locations and is separated from the plurality of first lines at the corresponding crossover locations by the release material; and

removing the release material from the corresponding crossover locations such that an air-gap is defined between each first line and the plurality of second lines at the corresponding crossover locations.

12. The method according to Claim 11,

wherein forming the first lines comprises depositing and etching a first metal layer,

wherein forming the release material pattern comprising depositing a second layer on the first lines, and

wherein forming the second lines comprises depositing a second metal layer on the release material pattern.

13. The method according to Claim 12,

wherein the first metal layer comprises at least one of Al and Cr,

wherein the second layer comprises at least one of photoresist, Si, and Al, and

wherein the second metal layer comprises TiW.

14. The method according to Claim 13, wherein removing the release material pattern comprises etching the release material without removing the first lines and the second lines.

15. The method according to Claim 11,

wherein forming the first lines comprises forming a plurality of spaced-apart support pads,

wherein forming the release material pattern comprises forming windows in a release material layer that expose upper surfaces of the spaced-apart support pads, and

wherein the plurality of second lines are formed such that each spaced-apart support pad contacts an associated first line.

16. The method according to Claim 11, further comprising forming a strengthening insulator on the plurality of second lines at the crossover locations.

17. The method according to Claim 11, further comprising forming a buried insulator layer over the first and second lines, wherein the buried insulator layer comprising a resin derived from B-staged bisbenzocyclobutene monomers.

18. The method according to Claim 17, further comprising forming a charge sensing region over the buried insulator layer such that the charge sensing region is separated from the first and second lines by the buried insulator layer.

19. The method according to Claim 11, wherein each pixel circuit of the integrated circuit includes an access transistor, and wherein the method further comprises forming the access transistor of each pixel circuit such that a first terminal of the access transistor contacts a corresponding first line, and a gate terminal of the access transistor contacts a corresponding second line.

20. The method according to Claim 19, wherein forming the access transistor comprises:

forming an amorphous silicon (a-Si:H) layer including a relatively undoped first region located over the associated first line, the first region being located between a doped second region and a doped third region; and

forming an optical filter island located over the first region, the optical filter island comprising at least three layers having at least two indexes of refraction and being arranged such that the optical filter island is reflective of a first radiation wavelength and transmissive of a second radiation wavelength.